

MATERIAL SIMULATION-BASED ELECTRONIC DEVICE PROGNOSIS

Loren Nasser, Robert Tryon, Animesh Dey

VEXTEC Corporation
750 Old Hickory Blvd, Bldg 2, Suite 270, Brentwood, TN 37027
615-372-0299
Lnasser@vextec.com; rtryon@vextec.com; adey@vextec.com

Abstract: Electronic failures can result in immediate system shutdown with no advanced fault or warning signal. As a device is operated thermal and/or mechanical loads are induced across the package. These loads are translated from the global package level to the localized interconnect level. VEXTEC's patent pending material-based simulation software accounts for real world interconnect variability and predicts probably of failure as a function of device operating time. This NAVAIR sponsored SBIR project demonstrated feasibility for using conventional, off-the-shelf sensing, to predict solder degradation due to thermal cycling as a means to prognosticate electronic device reliability.

Keywords: 1 electronics; 2 interconnect; 3 solder; 4 prognosis; 5 fatigue; 6 package; 7 thermal; 8 modeling

1. Introduction:

It is simply not practical to directly sense the degradation of electronic components. These damage states are usually structural and, due to their size, structural response signatures are not monitored on electronic components. For example, it would be both difficult and expensive to directly sense the cracking of a single emitter wire bond on a circuit board comprised of thousands of emitter wires. Yet, the failure of a single emitter wire can cause the failure of the device.

Conventionally the reliability of electronic devices is assessed using empirically-based models. Design of experiments is a commonly used tool in which the experimental conditions are systematically varied and a mathematical relationship is "fit" to the data that represents the influence of the conditions to the time or cycles to failure. However, one problem is the fact that there is so much variation in the time or cycles to failure that device life can only be conveyed in the form of a statistical average, such as mean time to failure (MTTF) or the mean time between failure (MTBF). These metrics are appropriate in the context of manufactured fleet lot reliability but they lack the fidelity for accurate representation of individual fielded device reliability.

Electronic device reliability prognosis requires that the analysis consider actual field

operating conditions for individual devices. These field conditions will be diverse sequences of loads and environments. Theoretically, empirical methods can be used to assess highly reliable systems if a statistically significant number of experiments were performed for every possible sequence of field conditions. As electronic components become smaller and they are used in more diverse environments with diverse sequencing, development of highly accurate empirically-based models is not practical.

VEXTEC has been developing a materials-based, large rotating component prognostic framework under DARPA, Air Force, and Navy program funding. At the foundation of this framework is VPS-MICRO™, which is fatigue crack initiation and total life prediction software. In early 2004, VEXTEC used VPS-MICRO™, under a series of blind validation tests facilitated by Pratt & Whitney, to successfully predict fatigue life for 5 alloys of Ti-6Al-4V material. Statistical analysis showed that the VPS-MICRO™ predictions were within 95% confidence bounds of the P&W test database.

This paper documents the work carried out under a Navy project to demonstrate the feasibility for using a similar prognosis framework for prediction of electronic system failure. Of specific concern to JSF readiness is the reliability of electronic power supplies. Power supply failure can result in immediate JSF system shutdown with no advanced fault or warning signals. According to JSF supplier sources, power supply systems are – compared to other electronic systems – highly susceptible to failure due to the high voltage and current conditions in which they routinely operate. Unlike mechanical systems, these electronic systems do not actively display conventional fault signals prior to failure.

Electronics, specifically power supplies, are reliant on the integrity of interconnects or solder bonds. The reliability of interconnects is a concern because it is widely expressed that fracture failures in solder joints accounts for up to 70% of failures in electronic components. The work under this project thoroughly documents the fact that interconnect or solder degradation and failure is attributed to thermomechanical fatigue mechanisms. Since VEXTEC has proven its fatigue life prediction methodology for large structural components, this project demonstrated a similar approach to predict small-scale interconnect reliability.

2. Solder Fatigue:

The most commonly used solder fatigue models are based on Coffin-Manson plastic strain equations developed for solder interconnects. Due to the low melting temperatures, most electronic devices operate at temperatures above solder creep thresholds. Since Coffin-Manson models do not explicitly address creep strains, specific solder models have been developed to incorporate creep (Knecht and Fox, 1991; Syed, 1997). All of the fatigue models in use today assume large scale similitude i.e., the structure (weld footprint or wire diameter) is large compared to the crack, the crack is large compared to the crack tip plastic zone and the crack tip plastic zone is large compared to the microstructure. These assumptions are fundamentally incorrect for today's small scale devices.

Energy-based solder fatigue models have been developed to account for the large crack size compared to the weld geometry (Liang et al., 1997) and Morris and Reynolds (1997) point out the importance of the size of the material microstructure compared to the size of the damage. Emitter bond wires are usually 300 to 500 microns in diameter and the metalization layer to which they are bonded have a thickness of 3 to 5 microns. With polycrystalline grain sizes as large as 150 microns, microstructural similitude cannot be assumed for crack initiation and growth. Figure 1 shows the relative size of the grains compared to the overall solder contact area.

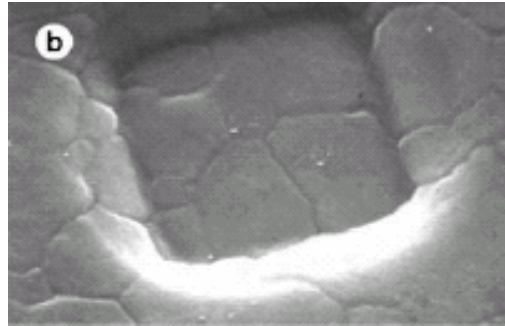


Figure 1. Few material grains make up a typical package interconnect.

None of the previously described fatigue models account for the large scatter in the solder weld properties. The nature of the packaged components and variability within the assembly process creates large variations in the solder welds for even the strictest manufacturing tolerances. The very small size of the welds causes variation of the weld footprint from weld to weld. In addition, the microstructural development of the weld is greatly controlled by rate of cooling from the melt stage. Some of the components within a package are specifically designed with heat sinks for thermal management during operation. These heat sinks are activated during the assembly process by the heat of the welding although they may not have been specifically designed for this purpose. This heat transfer action causes uneven cooling of the welds from component to component and uneven cooling of the different emitter bonds within a single component. Conventionally used electronic device reliability prediction, largely empirically derived, do not account for this real world variability. Thus, variation in the geometry and material properties of the weld must be considered in order to prognosticate reliability accurately.

Industry research indicates that thermo-mechanical fatigue damage mechanisms in Sn/Pb solder as time dependent (creep) shear stress induced cracks initiate and propagate in the solder near the intermetallic interface. The fatigue response of the solder changes due to instability (coarsening) of the microstructure. Although, both intergranular and transgranular fracture surfaces are observed, depending on loading and temperature, transgranular appears to predominate.

VPS MICRO™ is a probabilistic fatigue prediction capability that explicitly models fatigue damage (dislocations, slip band, small crack and long cracks) and the damage interaction with material microstructural features (crystallographic planes, phase boundaries, grain boundaries, etc.). VPS MICRO™ uses Monte Carlo techniques to simulate damage accumulation on a cycle by cycle basis. Monte Carlo reliability techniques are used so that model parameters such as loading, temperature and microstructure can simulate real world conditions by varying randomly with time. The VEXTEC overall electronics package prognosis approach is depicted in Figure 2.

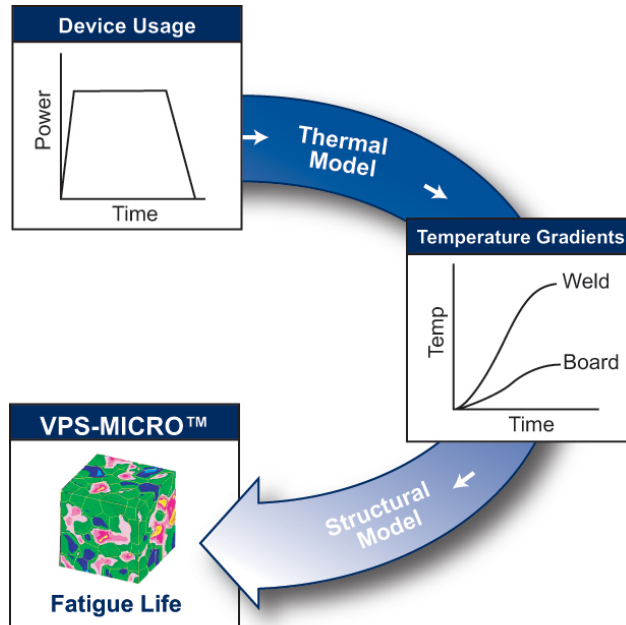


Figure 2. VEXTEC overall prognosis approach.

3. Electronic Prognosis Issues:

The developed prognosis model had to incorporate mission sequencing (i.e.: turning the device on/off and creating thermal swings), geometric design parameters (i.e.: variation in footprint of the solder welds), and material parameters (i.e.: intermetallic interface zone thickness variation).

Electronic device operating principles require that the design parameters be accurately coupled. In order to assess the physical changes in variables at the electronic system level, appropriate system reliability modeling techniques must be applied. For example, temperature gradients are caused by the complex heat transfer characteristics within the device. A chip consists of material layers of various makeup and thicknesses. Some layers radiate heat while others absorb it. Still further, neighboring chips and devices influence the thermal characteristics of the chip as well. Computational analysis techniques such as finite element analysis (FEA) are often used to assess the complex thermal environment during design. Such an environment can be simulated as a temporal thermal mission with start-up and shutdown transients along with steady state conditions. Electronics industry research indicates that the highest stresses imposed within the device are the result of temperature gradients created during on/off transients. The thermal stresses can also be combined with the purely mechanically induced stresses (such as vibration) within the FEA to predict the overall device stresses. The resulting stress prediction becomes the basis for VPS-MICRO™ cyclic life prediction.

The electronics industry routinely combines physics-based thermal or vibration models with empirically-based fatigue models to make a rough order of magnitude prediction of device life. However, the traditionally used semi-empirical approach lacks the required fidelity to be useful in the prognosis of thermo-mechanical fatigue for individual components. Lau and Pao (1997) point out some of the issues for using the current semi-empirical MTTF or MTBF approach. These issues, along with VEXTEC's methodology for overcoming these, are as follows:

Geometry: Dimensional variation of components within electronic packages can be of several orders of magnitude, e.g. a 0.08 x 0.1 mm solder bump versus a 150 x 150 mm Printed Wiring Board (PWB). This necessitates breaking down the numerical analysis into multi-scale (local and global) analyses. Also there is a difference in the actual and simplified geometries of the component or interconnect. For example, the actual geometry of a solder joint depends on a number of parameters such as solder-paste volume, reflow temperature and flux, which can result in a wide range of different shapes. Oversimplification may eliminate geometric discontinuities or defects, which may be intimately associated with a significant part of fatigue life. To address geometry issues, VEXTEC has developed multi-scale finite element models to relate the global stresses and strains caused by the thermal mismatch between the electrical device and the circuit board to the local stresses and strains in the intermetallic solder layers. These methods allow for statistical variations in the complex geometry at the global, local and any intermediate level.

Meshing: Electronic packages are bi-material and tri-material bonded edges and interfaces. Stress concentrations cause interfacial damage or cracks to initiate. Capturing detailed stress-strain distributions with reasonable meshes near these concentrations is difficult. Also, many materials used in packaging are of thin layer shapes, such as thin and thick films. Thus, aspect ratio becomes a problem and a large number of elements are required to accurately model the behavior of these thin layers. The multi-scale finite element models used by VEXTEC addresses meshing issues by incorporating a representative volume element (RVE) approach in which different size scales are modeled with separate RVE's. These RVEs are properly linked using "nested models". This approach allows for small regions of highly concentrated stresses and strains to be modeled with separate RVE's and then linked to the next higher size scale.

Material Properties: Properties of internal solder layers, such as intermetallic regions between the solder and silicon substrate, are not well known. Most properties are temperature and time dependent. The mechanical behavior of a solder joint, for example, depends on strain rate, temperature, cooling rate, loading history and microstructure. Mechanical properties measured using relatively large scale and bulk specimens generally are not the same as those for actual solder interconnects. To address material property issues, VPS MICRO™, a physics-based fatigue analysis approach models the interaction of the fatigue damage with the material microstructure. The material microstructure is explicitly modeled at the crystalline level; no bulk assumptions are made.

4. Prognosis Approach:

Figure 3 presents an overview of VEXTEC's Phase I feasibility demonstration. Temperature cycling produces stresses at the global component level that are translated to local stresses at the material microstructural level. VEXTEC modified the VPS-MICRO™ fatigue analysis approach for use with electronic materials. VPS-MICRO™ was used to predict weld probability of failure as a function of system usage. Further, the approach used to predict the response of a board with many welds and associated failure interrelationships.

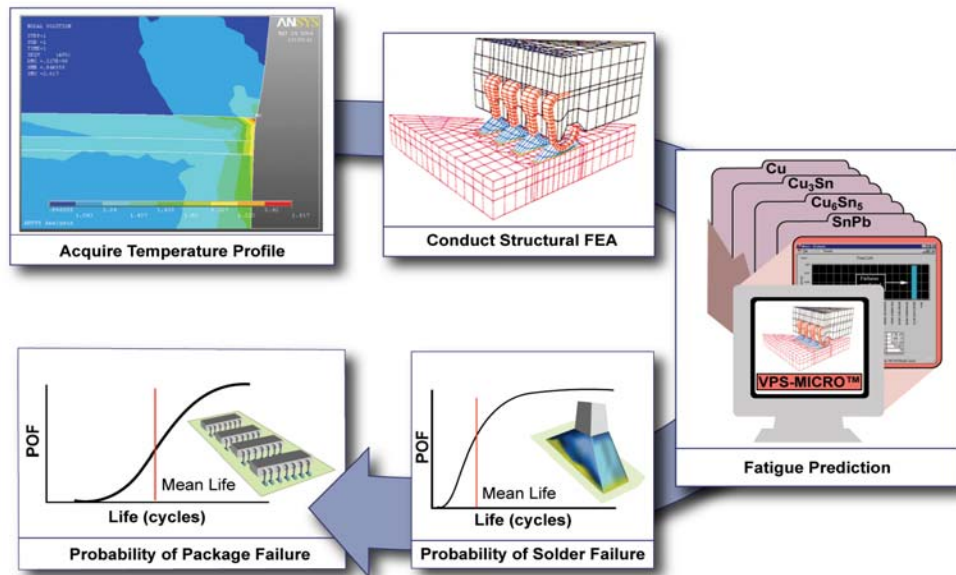


Figure 3. Prognosis demonstration approach.

4.1 Global Modeling:

Conventional FEA analysis is incorporated within the VEXTEC analysis approach. SRI (Menlo Park, CA) performed a thermo-mechanical stress analysis for a J-leaded device for several different packages with different material layering combinations. Under this project an Alloy 42 lead is soldered to a FR-4 board with a copper metalization layer. For the feasibility demonstration described later in this paper, only the corner joint was simulated since it had the highest stresses and can be considered a representative example.

4.2 Local Modeling:

Fatigue failure is a localized, material-driven process. An extensive amount of research has been conducted as to how and why cracks initiate and grow within solder connections. This knowledge was adopted within the developed local simulation modeling approach. High stresses are translated from global loadings to the local material. In particular these stresses exist at the interface between the copper lead and the

solder. These localities are of compounded significance due to the existence of a complex microstructure of intermetallic layers between the copper and the solder. When molten Sn-Pb solder contacts the lead, intermetallic compounds (IMC) are formed between the solder and the lead. To model the complex stress state of the microstructure at the copper/solder interface, two dimensional ANSYS finite element models were created under this project by VEXTEC for the copper/intermetallic/solder region. Because the thickness of the intermetallic layers change with time, a series of finite element models were created for various Cu_3Sn and Cu_6Sn_5 thicknesses to simulate this real world variability. Figure 4 shows the example FEA model for 4 microns of Cu_3Sn and 7 microns of Cu_6Sn_5 used for demonstration purposes. The bottom layer shown in the model is copper.

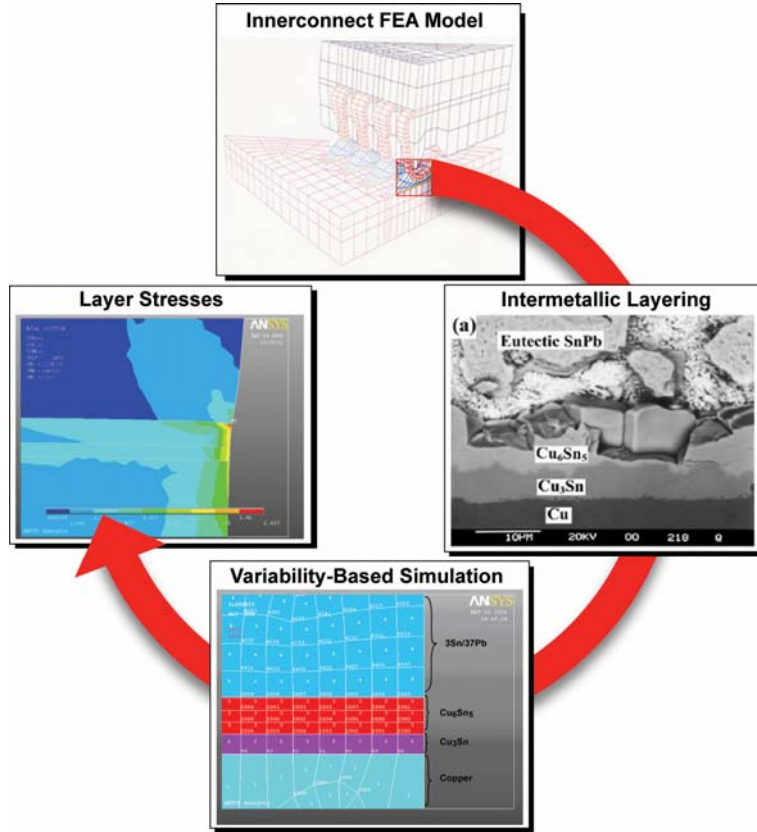


Figure 4: Global stress translated to local microstructure through simulation of intermetallic region.

variability. Figure 4 shows the example FEA model for 4 microns of Cu_3Sn and 7 microns of Cu_6Sn_5 used for demonstration purposes. The bottom layer shown in the model is copper.

4.3 System Reliability.

Response surface techniques are used to combine the global and local stress analysis with the microstructural growth kinetics to create a simple mathematical equation of the complex relationship between temperature, dwell time and the stress at the solder joints.

$$\sigma = \frac{T}{256} (c_1 + c_2 d_1 + c_3 d_2 + c_4 d_1^2 + c_5 d_2^2 + c_6 d_1 d_2)$$

where:

$$d_n = \left(D_n e^{\left(\frac{-Q_n}{kT} \right) t} \right)^{\frac{1}{2}} \quad (1)$$

$n = 1$ for Cu_6Sn_5

$n = 2$ for Cu_3Sn

Where σ is the stress in the solder joint, T is the temperature, t is the cumulative time at temperature, d_n are the thicknesses of the intermetallic layers, c_i are the least squares fit

coefficients and D_n , Q_n and k are material properties.

5. Electronic Prognosis Demonstration:

For feasibility demonstration purposes, an individual solder connection was simulated as being thermally cycled between room temperature and 256 F over 15 minute dwell periods. During actual device operation these temperature inputs will come from conventional thermocouple sensors mounted on the device being analyzed. If a thermocouple can not be mounted on or near the device then conventionally sensed voltages or currents can be translated to board temperature through currently available thermal modeling approaches. Either way, this prognosis approach builds upon state of awareness capabilities in existence today.

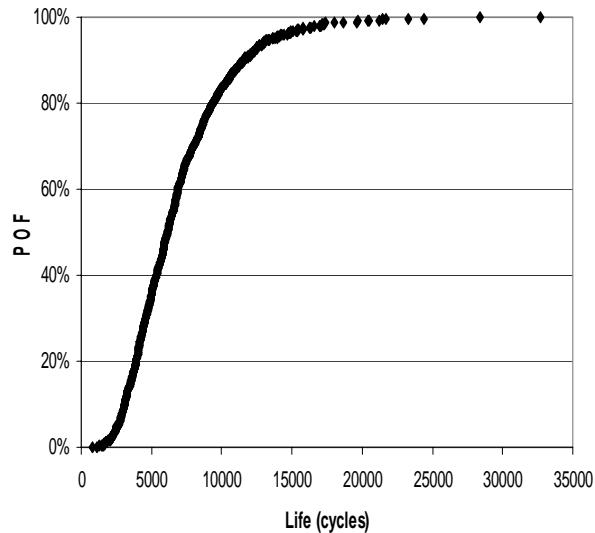


Figure 5: Thermal cycling induced failure prognosis for an individual solder joint.

Based on the industry identified driving mechanisms that cause solder materials to degrade and initiate cracks, VPS-MICROTM fatigue software was used to predict solder joint life. This feasibility demonstration found that a single, commonly used, simulated solder bond was predicted to have a mean life of approximately 7000 cycles (Figure 5).

5.1 Device with Many Interconnects:

Electronic devices are typically attached to circuit boards or housings through multiple solder connections. To prevent against excessive heating, electronic OEMs use finite element modeling to predict the stresses imposed on device interconnects during design. This Phase I showed how these global stresses can be translated to the material microstructural level, and that these stresses vary for each interconnect location due to the realistic simulation of a thermal gradient across the device. VPS-MICROTM software was used to prognosis the life expectation difference for an interior solder location compared to an edge solder location. Using a standard industry system reliability approach, it was demonstrated that a thermally cycled device with 28 individual solder connections (7 per side, 4 edge joints) was predicted to have a mean life of 2554 cycles.

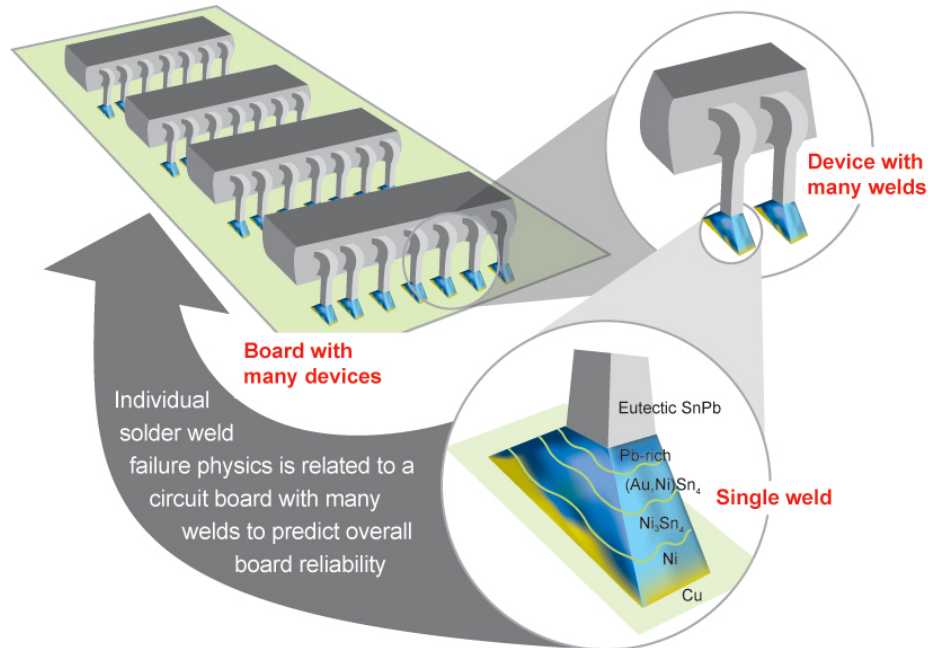


Figure 6. Package reliability predicted through a systems approach.

5.2 Electronic Package with Many Devices:

An electronic system, such as a power supply, will be comprised of many individual devices. In order to demonstrate package prognosis proof of concept, a circuit board with 20 individual devices (each with 28 solder joints) was thermally cycled through the previously described simulation process (Figure 6). Just as expected in actual operation, a thermal gradient was simulated across the board causing the thermally induced stresses to vary from device to device. This demonstration predicted that the board, with 20 devices, will have a mean life of 1283 cycles which was lower than the life predicted for any single device considered alone.

6. Summary:

This SBIR Phase I has successfully demonstrated how VPS-MICRO™ fatigue simulation can be used for electronics systems prognosis. Electronics, specifically power supplies, are reliant on the integrity of interconnects. Industry reliability data indicates that fracture failures in solder joints accounts for up to 70% of failures in electronic digital devices. Electronics industry specific thermal models along with generalized structural finite element software can be used with VPS-MICRO™ software to predict solder fatigue response.

Phase I used simulated, conventionally sensed thermal cycling data, from room temperature to 256 F, as input to the VEXTEC prognosis approach. It was demonstrated that individual interconnect life as well as that for a device or chip with many interconnects could be prognosed. Thereafter life prognosis was demonstrated for a circuit board with many devices that also considered the realistic simulation of a thermal gradient was applied across the board.

This paper identifies that the inherent weaknesses of currently used empirically-based approaches such as MTTF or MTBF have been avoided in the VEXTEC prognosis methodology. One day this prognosis approach will be used to predict board or device degradation prior to failure. Such capability is non-existent today within aircraft systems (as an example). Today operational performance is assured through systems redundancy and through the implementation of extremely conservative maintenance practices. Redundancy is inefficient, adds weight and takes up valuable real estate within the aircraft. Conservative maintenance results in increased downtime and higher operational costs due to excessive inspections, tear-downs and replacements. This prognosis technology will mitigate the need for electronic redundancy and allow for maintenance for cause decisions.

References:

- [1] Tryon, R.G., "Onboard, Prognostic Micro-structural Reliability Tool for Mechanical Systems," DARPA Contract DAAH01-01-C-R127, 2001
- [2] Knecht, S., Fox, L. (1991) "Integrated matrix creep: application to accelerated testing and lifetime predictions, "Solder joint reliability theory and applications," Van Nostrand Reinhold, New York.
- [3] Liang, J., Gollhart, N., Lee, P. S., Heinrich, S., Schroeder, S (1997) "An integrated fatigue life prediction methodology for optimum design and reliability assessment of solder inter-connectors," Advances in Electronic Packaging, Vol 2.
- [4] Morris, J. W., Reynolds, H. L. (1997) "The influence of Microstructure on the mechanics of eutectic solders," Advances in Electronic Packaging, Vol 2.
- [5] Lau, J.H. and Pao, Y.H. (1997). Solder Joint Reliability of BGA, CSP, Flip Chip and Fine Pitch SMT Assemblies, McGraw Hill, NY.

Biography:

Loren Nasser is COO responsible for day to day operations at VEXTEC Corporation. He has been actively involved in the development of reliability prediction software within the aerospace, electronic and automotive marketplace. He has an M.S. in engineering science from the University of Tennessee and B.S. in mechanical engineering from Rose-Hulman Institute of Technology.

Robert Tryon is co-founder and CTO at VEXTEC Corporation. He has lead the development of the patent-pending "VPS-MICRO" software. He served as principal investigator on VEXTEC's DARPA and NAVAIR prognosis technology development projects and has served in a similar role on numerous other projects. He received a Ph.D. in structural engineering from Vanderbilt University and an M.S. and B.S. in mechanical engineering from Rose Hulman Institute of Technology.

Animesh Dey is co-founder and CPDO at VEXTEC Corporation. He has been involved in the development of reliability software for the automotive industry and has served in a similar role on numerous other projects. He received a Ph.D. and M.S. in structural engineering from Vanderbilt University and B.S. from the Indian Institute of Technology.